SC11867MP

IN THE CLAIMS:

Please cancel claims 19-28 and amend claims 1, 4, 12 and 15, as follows:

1. (currently amended) A stacked multichip package, comprising:

a base carrier having a top side and a bottom side;

a bottom integrated circuit die having a bottom surface attached to the base carrier top side, and an opposing, top surface, the top surface having a peripheral area including a plurality of first bonding pads and a central area;

a bead formed on the top surface of the bottom die between the peripheral area and the central area, wherein the bead does not extend to the first bonding pads;

an adhesive material formed in the central area on the top surface of the bottom die, the adhesive material being surrounded by the bead; and

a top integrated circuit die having a bottom surface, wherein the top die is positioned over the bottom die and the bottom surface of the top die is attached to the top surface of the bottom die via the adhesive material, wherein the bead maintains a predetermined spacing between the bottom die and the top die and wherein the top die and the bottom die are of similar size and shape as the bottom die.

2. (original) The stacked multichip package of claim 1, wherein the bottom die is attached to the base carrier with a first adhesive material layer.

3. (canceled)

4. (currently amended) A ~~The~~ stacked multichip package ~~of claim 1~~, comprising:

a base carrier having a top side and a bottom side;

a bottom integrated circuit die having a bottom surface attached to the base carrier top side, and an opposing, top surface, the top surface having a peripheral area including a plurality of first bonding pads and a central area;

a bead formed on the top surface of the bottom die between the peripheral area and the central area, wherein the bead does not extend to the first bonding pads;

an adhesive material formed in the central area on the top surface of the bottom die, the adhesive material being surrounded by the bead; and

a top integrated circuit die having a bottom surface, wherein the top die is positioned over the bottom die and the bottom surface of the top die is attached to the top surface of the bottom die via the adhesive material, wherein the bead maintains a predetermined spacing between the bottom die and the top die and wherein the top die is larger than the bottom die.

5. (original) The stacked multichip package of claim 1, wherein the bead comprises epoxy.

6-7. (canceled)

8. (previously presented) The stacked multichip package of claim 1, wherein the adhesive material comprises epoxy.

9. (previously presented) The stacked multichip package of claim 1, wherein the bottom die is electrically connected to the base carrier with first wires, the first wires having first ends electrically connected to the first bonding pads and second

ends electrically connected to first leads on the top side of the base carrier.

10. (original) The stacked multichip package of claim 9, wherein the top die includes a plurality of second bonding pads located in a peripheral area on a top surface of the top die and wherein the top die is electrically connected to the base carrier with second wires, the second wires having first ends electrically connected to the second bonding pads and second ends electrically connected to second leads on the top side of the base carrier.

11. (previously presented) The stacked multichip package of claim 10, further comprising an encapsulant covering the first and second dies, the first and second wires, and at least a portion of the top side of the base carrier.

12. (currently amended) A stacked multichip package, comprising:

a base carrier having a top side and a bottom side, the top side including a plurality of first leads and a plurality of second leads;

a bottom integrated circuit die having a bottom surface attached to the base carrier top side, and an opposing, top surface, the top surface having a peripheral area including a plurality of first bonding pads and a central area, wherein the bottom die is electrically connected to the base carrier with first wires, the first wires having first ends electrically connected to the first bonding pads and second ends electrically connected to the first leads;

a bead formed on the top surface of the bottom die between the peripheral area and the central area, wherein the bead does not extend to the first bonding pads;

an adhesive material formed in the central area on the top surface of the bottom die, the adhesive material being surrounded by the bead;

a top integrated circuit die of similar size and shape as the bottom die, the top die having a bottom surface, wherein the top die is positioned over the bottom die and the bottom surface of the top die is attached to the top surface of the bottom die via the bead and the adhesive material, and the bead maintains a predetermined spacing between the bottom die and the top die, and wherein the top die includes a plurality of second bonding pads located in a peripheral area on a top surface thereof and wherein the top die is electrically connected to the base carrier with second wires, the second wires having first ends electrically connected to the second bonding pads and second ends electrically connected to the second leads; and

an encapsulant covering the first and second dies, the first and second wires, and at least a portion of the top side of the base carrier.

13. (original) The stacked multichip package of claim 12, wherein the bottom die is attached to the base carrier with a first adhesive material layer.

14. (canceled)

15. (currently amended) ) A ~~The~~ stacked multichip package ~~of claim 13~~, comprising:

a base carrier having a top side and a bottom side, the top side including a plurality of first leads and a plurality of second leads;

a bottom integrated circuit die having a bottom surface attached to the base carrier top side with a first adhesive material layer, and an opposing, top surface, the top surface having a peripheral area including a plurality of first bonding pads and a central area, wherein the bottom die is electrically connected to the base carrier with first wires, the first wires having first ends electrically connected to the first bonding pads and second ends electrically connected to the first leads;

a bead formed on the top surface of the bottom die between the peripheral area and the central area, wherein the bead does not extend to the first bonding pads;

an adhesive material formed in the central area on the top surface of the bottom die, the adhesive material being surrounded by the bead;

a top integrated circuit die having a bottom surface, wherein the top die is positioned over the bottom die and the bottom surface of the top die is attached to the top surface of the bottom die via the bead and the adhesive material, and the bead maintains a predetermined spacing between the bottom die and the top die, and wherein the top die includes a plurality of second bonding pads located in a peripheral area on a top surface thereof and wherein the top die is electrically connected to the base carrier with second wires, the second wires having first ends electrically connected to the second bonding pads and second ends electrically connected to the second leads, wherein the top die is larger than the bottom die; and

an encapsulant covering the first and second dies, the first and second wires, and at least a portion of the top side of the base carrier.

16. (original) The stacked multichip package of claim 13, wherein the bead comprises epoxy.

17. (original) The stacked multichip package of claim 16, wherein the adhesive material comprises epoxy.

18. (original) The stacked multichip package of claim 13, wherein the predetermined spacing between the top die and the bottom die maintained by the bead is sufficient to protect the electrical connections between the first wires and the first bonding pads from being damaged by the attachment of the top die to the bottom die.

19-28. (canceled)